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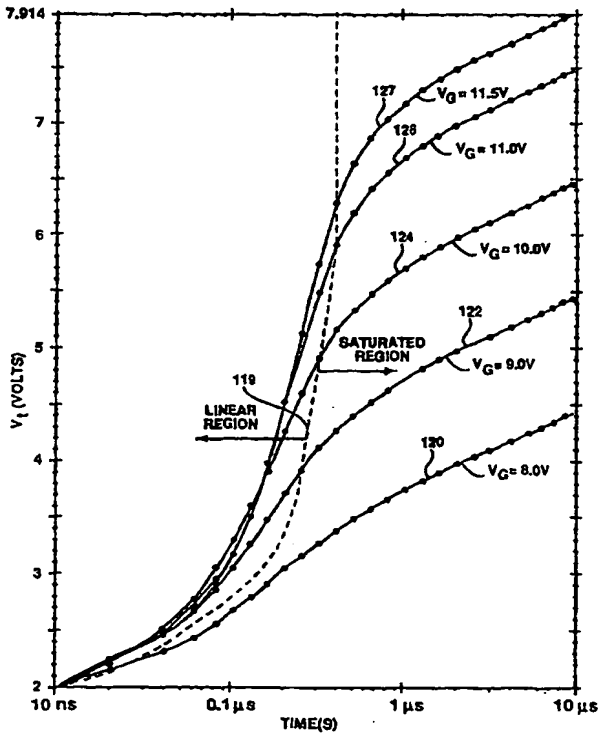
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(54) Title: METHOD AND CIRCUITRY FOR STORING DISCRETE AMOUNTS OF CHARGE IN A SINGLE MEMORY ELEMENT

(57) Abstract

A method and circuitry for programming a memory cell to one of at least three amounts of charge. The amount of charge placed in the memory cell is increased by increasing the voltage level of a programming pulse applied to the memory cell.



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METHOD AND CIRCUITRY FOR STORING DISCRETE AMOUNTS OF
CHARGE IN A SINGLE MEMORY ELEMENT

FIELD OF THE INVENTION

The present invention relates to the programming of memory cells. More particularly, the present invention relates to a method and circuitry for programming flash memory cells to store discrete amounts of charge representing multiple bits of data in a single memory cell.

BACKGROUND

Nonvolatile semiconductor memories use a variety of semiconductor memory cell designs. One type of memory cell uses an electrically isolated floating gate to trap charge. A variety of mechanisms can be used to insert charge into the floating gate and to pull charge from it. Electron tunneling can be used both to inject charge and to pull charge off the floating gate of a memory cell. Hot electron injection is another mechanism for inserting charge into a floating gate of a memory cell. Other nonvolatile semiconductor memories use a trapping dielectric to insert or remove charge from between the control gate of a memory cell and silicon.

An attractive feature of nonvolatile semiconductor memories is their ability to retain data when powered off. Another attractive feature of nonvolatile semiconductor memories is their ability to store analog data. This permits storage of multiple bits of data in a single memory cell, which is sometimes called multistate storage.

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There are prior patents that discuss multistate storage. U.S. Patent No. 5, 043,940 of Harrari for FLASH EEPROM MEMORY SYSTEMS HAVING MULTISTATE STORAGE CELLS ("Harrari") defines four states in terms of the threshold voltage V_t of a split-channel memory cell. Using these four states, Harrari is able to store two bits of data per memory cell by applying multiple programming pulses to each memory cell.

U.S. Patent No. 5,163,021 of Mehrota et al. for MULTI-STATE EEPROM READ AND WRITE CIRCUITS AND TECHNIQUES ("Mehrota") describes multilevel programming of split-channel memory cells in greater detail. Like Harrari, Mehrota defines four states in terms of memory cell threshold voltage. Mehrota describes programming multiple memory cells in parallel. A program pulse is applied to a group of cells simultaneously. Each cell is then program verified and those cells that are properly programmed are protected from further programming. Program pulses are applied until all memory cells in the group are properly programmed. Mehrota discloses using the same voltage levels for each subsequent programming pulse.

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SUMMARY AND OBJECTS OF THE INVENTION

An object of the present invention is to provide a method and circuitry for storing discrete amounts of charge in a memory cell within a reasonable time period.

Another object of the present invention is to provide a method and circuitry for rapidly programming memory cells to allow storage of multiple bits of data in a single memory cell.

Another object of the present invention is to provide a method of accurately programming memory cells to selected states, which represent patterns of multiple data bits.

These and other objects of the invention are met by a method and circuitry for programming a memory cell to one of at least three amounts of charge. The amount of charge placed in the memory cell is increased by increasing the voltage level of a programming pulse applied to the memory cell.

Other objects, features, and advantages of the present invention will be apparent from the accompanying drawings and the detailed description that follows.

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BRIEF DESCRIPTION OF THE DRAWINGS

The present invention is illustrated by way of example and not limitation in the figures of the accompanying drawings in which like references indicate similar elements and in which:

Figure 1 is a block diagram of a personal computer.

Figure 2 is a block diagram of a memory device.

Figure 3 is a schematic diagram of a portion of a memory array.

Figure 4A illustrates four states defined by different threshold voltages of a nonvolatile memory cell.

Figure 4B illustrates four states defined by different drain currents of a nonvolatile memory cell.

Figure 5 is a flow diagram of a method of programming in parallel multiple memory cells.

Figure 6 graphs threshold voltage versus time for various gate voltages.

Figure 7 graphs threshold voltage versus time for various drain voltages.

Figure 8 graphs threshold voltage versus time for various drain voltages.

Figure 9 illustrates the number of programming pulses required to program a group of memory cells versus state width.

Figure 10 is a flow diagram of a method of individually programming memory cells to store differing amounts of charge.

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Figure 11 is a block diagram of a circuit for sensing and verifying the programming of a memory cell storing multiple bits of data.

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DETAILED DESCRIPTION

Figure 1 illustrates in block diagram form a computer system. The computer system includes a central processing unit ("CPU") and a monitor for visually displaying information to a computer user. A keyboard allows the computer user to input data to the CPU. By moving a mouse the computer user is able to move a pointer displayed on the monitor. Memory stores data used by the CPU. Nonvolatile semiconductor memory device 20 is one type of memory accessed by the CPU. Nonvolatile semiconductor memory 20 has the advantage of retaining data when powered off.

Figure 2 illustrates in block diagram form nonvolatile memory device 20, which is fabricated on a single semiconductor substrate. Memory device 20 stores data using nonvolatile memory cells within memory array 22. The threshold voltages of the nonvolatile memory cells can be altered during programming, thus permitting storage of analog voltage levels. Memory array 22 may include any type of memory cell with programmable threshold voltages, such as memory cells with trapping dielectrics or floating gates. In one embodiment, memory array 22 is comprised of flash memory cells.

Methods of programming memory cells to store discrete amounts of charge will be described in more detail herein below. Briefly described, these methods use multiple programming pulses to place differing discrete amounts of charge within the memory cells. The amount of charge placed

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within each memory cell is varied by varying the gate or wordline voltage level during programming pulses. Placing differing discrete amounts of charge in each memory cell permits storage of multiple bits of data in a single memory cell. These methods are applicable to both nonvolatile memory cells, such as used in flash EPROMs, and volatile memory cells, such as used in dynamic random access memories (DRAMs).

I. Memory Device Overview

Prior to beginning that detailed discussion of programming, consider again memory device 20 to which the methods are applied. V_{pp} is the erase/program power supply for memory device 20. In the absence of a high voltage level on the memory cells, memory device 20 acts as a read only memory. The data stored at an address indicated by address lines 24 is read from memory array 22 and is output to the external user via data lines 26.

X decoder 28 selects the appropriate row within memory array 22 in response to address signals applied to address lines 24. For this reason, X decoder 28 is also called row decoder 28. Similarly, Y decoder 30 selects the appropriate column within memory array 20 in response to address signals from address lines 24. Because of its function, Y decoder 30 is also called column decoder 30.

Data output from memory array 22 is coupled to Y decoder 30, which passes the data on to sensing circuitry 32. Sensing circuitry 32 determines

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the state of data presented to it using reference cell array 34. Sensing circuitry 32 then passes the results of its analysis back to Y decoder 30.

In an embodiment of memory device 20, control engine 36 controls the erasure and programming of memory array 22. Control engine 36 also controls the programming of multilevel cells, which will be described in detail herein below. In one embodiment, control engine 36 includes a processor, that is controlled by microcode stored in on-chip memory. However, the particular implementation of control engine 36 does not affect the present method of programming of multilevel cells.

Control engine 36 manages memory array 22 via control of row decoder 28, column decoder 30, sensing circuitry 32, reference cell array 34 and voltage switch 38. Voltage switch 38 controls the various voltage levels necessary to read, program and erase memory array 22. V_{CC} is the device power supply and V_{SS} is ground. V_{PP} is the program/erase voltage, which must be high in order to program or erase data stored within memory array 22. V_{PP} may be externally supplied or internally generated.

User commands for reading, erasure, and programming are communicated to control engine 36 via command interface 40. The external user issues commands to command interface 40 via three control pins: output enable OEB, write enable WEB, and chip enable CEB.

Programming memory cells according to the present methods requires some understanding of the organization of memory array 22. Figure 3 illustrates in detail a portion 22a of memory array 22. Portion 22a

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includes six single field effect transistor floating gate memory cells 50, 52, 54, 56, 58, and 60. This type of memory cell is shown solely for illustration purposes. Other types of memory cells may also be programmed to multiple states using the present methods. For example, multiple transistor memory cells and memory cells that use a trapping dielectric to shift the threshold voltage of the memory cells may both be programmed using the present methods. Additionally, volatile memory cells, such as those used in DRAMs, could be programmed using the present methods.

Memory cells 50, 52, 54, 56, 58, and 60 are formed at the intersections of word lines 62 and 64 and bit lines 66, 68, and 70. Word lines 62 and 64 are also referred to as X lines or row lines. This is because each wordline is coupled to X decoder 28. Each wordline is also coupled to all memory cell gates in a particular row. For example, word line 62 is coupled to the gates of memory cells 50, 52, and 54. Bit lines 66, 68 and 70 are also referred to as Y lines or column lines because they are coupled to Y decoder 30. Each bitline is coupled to all memory cell drains in a particular column. For example, bitline 68 is coupled to the drains of memory cells 52 and 58. The sources of all memory cells in a row are coupled to a local source line. The sources of memory cells 50, 52 and 54 are coupled to local source line 72, while the sources of memory cells 56, 58 and 60 are coupled to local source line 74. Local source lines 72 and 74 are also coupled to common source line 76, which is coupled to voltage switch 38. Common source line 76 thus provides a mechanism for

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applying voltages to the sources of all memory cells within a block of memory array 22.

Together the bitlines, wordlines, and the common source line provide a means of applying to the memory cells the voltages necessary for programming, erasing, and reading memory cells within array 22. Memory cells 50, 52, 54, 56, 58 and 60 are erased via Fowler-Nordheim tunneling by applying approximately zero volts to memory cell gates via wordlines 62 and 64, allowing bitlines 66, 68 and 70 to float, and tying memory cell sources to approximately 12 volts via common source line 76. Memory cells 50, 52, 54, 56, 58, and 60 can also be erased via negative gate erase by applying -10 volts to memory cell gates, allowing the drains to float, and coupling the sources to 5 volts. Within flash memory arrays, an entire block of memory cells is erased at once. Memory cells are read, that is to say their states are sensed, by applying one to seven volts to wordlines 62 and 64, approximately one volt to bitlines 66, 68 and 70 and allowing common source line 76 to float. Memory cells 50, 52, 54, 56, 58, and 60 are programmed via hot electron injection by applying a source voltage V_S to common source line 76, applying a drain voltage V_D to bitlines 66, 68, and 70 such that the bitline voltage level is 5-7 volts above source line 76; i.e., setting V_{DS} to 5-7 volts, and applying a voltage level to wordlines 62 and 64 sufficient to change the amount of charge stored by the memory cells being programmed. Other voltage levels also can be used to program memory cells. As used herein, "programming pulse" refers to the

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combination of voltages applied to the bitline, sourceline, and wordline of a memory cell to shift its threshold voltage by changing the amount of charge stored in the memory cell.

A group of memory cells are selected for programming and reading by coordinating the control of wordline and bitline voltages. To illustrate, assume that memory cell 50 is to be programmed. The gate voltage for memory cell 50 is brought to, and held at, the appropriate level via wordline 62, which also applies the same voltage to the gate of memory cells 52 and 54. Local source line 72 applies the same voltage to the sources of all three memory cells. Memory cell 50 is programmed by pulsing the voltage on its drain by pulsing the voltage on bitline 66, while bitlines 68 and 70 are held near ground and wordline 62 is held at a high enough voltage to develop a desired electric field across the gate oxide of memory cell 50. Thus, only memory cell 50 is programmed. The duration of a programming pulse within memory array 22 is controlled by the duration of the high voltage on the selected bitline, that is to say, by the drain voltage.

As stated previously, programming and erasure of a memory cell alters its threshold voltage and the drain current conducted by the memory cell during sensing. Possible threshold voltages in a nonvolatile memory cell range from a lower limit of approximately 1.5 volts to an upper limit of approximately 7.0 volts. The lower limit of the programming range, or programming window, is constrained by erase times and gate disturb voltages. The upper level of the programming window is constrained by

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drain disturb voltages and bake charge loss. The programming window permits nonvolatile memory cells to store more than one bit of data.

For memory cells storing more than one bit of data there is not a one to one correspondence between the number of memory cells within array 22 and the number of bits of data stored by array 22. Thus, the phrases "memory cell" and "bit" are not used synonymously herein. "Memory cell" refers to a physical device, such as a transistor illustrated in Figure 3, and "bit" or "bits" refers to the logical data stored within a memory cell.

The number of bits, B, stored within a nonvolatile memory cell is related to the number of states, S, by the equation $S = 2^B$, where B is not restricted to integer values. The number of states that could be stored within a nonvolatile memory cell is limited in practice by the ability to place states and to distinguish between those states at some later time. Thus, if the sensing circuitry can detect the difference of a single electron, then states may be defined in terms of a single electron. States may be defined in terms of memory cell threshold voltage level or drain current. Memory cell threshold voltage V_t , and drain current I_D are approximately related to each other by the expression:

$$I_D \propto G_m \times (V_G - V_t) \text{ for } V_D > V_G - V_t$$

G_m is the transconductance of the memory cell;

V_G is the memory cell gate voltage;

V_D is the memory cell drain voltage; and

V_t is the memory cell threshold voltage.

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For memory cells storing multiple bits of data, each of the possible patterns of bits represents one state. In effect, the cell is storing base S data, where S is the number of states the cell is capable of storing. The bit pattern results from decoding the state data of one or multiple cells. For example, for memory cells storing two bits of data there are four bit patterns: 00, 01, 10, and 11. Each of these bit patterns is represented by a state. The particular state represented by a particular pattern of bits depends upon the type of coding used. Two commonly used types of coding are Gray coding and binary coding. The type of coding used does not effect the present methods of programming.

States may be defined in a variety of ways. They may be defined in terms of a range of threshold voltages V_t , a range of drain currents I_d , or a range of charge.

II. Exact Placement Algorithms For Programming Multiple States

Exact placement algorithms program each nonvolatile memory cell to a destination state that is defined by a range of threshold voltages V_t , or drain currents I_d or an amount of charge. Figures 4A and 4B illustrate two definitions of four states for a nonvolatile memory cell storing 2 bits of data. According to the definition of Figure 4A, states 0, 1, 2, and 3 each occupy a range of threshold voltages, V_t . The state representing the lowest threshold voltage, state 0, is achieved by erasing the memory cell. The other three states, states 1-3, are achieved by programming the memory cell. Figure

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4B defines four states in terms of ranges of drain current. The state representing the greatest amount of drain current, state 0, is achieved by erasing the memory cell. The other three states, states 1-3, are achieved by programming.

When exactly placing states, however defined, the designer may choose to program multiple memory cells in parallel; i.e., simultaneously, or to program each memory cell individually. Programming multiple cells in parallel regardless of their destination states requires using multiple program pulses to avoid overshooting states. In contrast, a single programming pulse may be used when memory cells are programmed independently of each other. Both methods of exact placement account for program variation caused by most sources of variation, such as V_{pp} variation, temperature variation, and cell-to-cell variation. Additionally, exact placement methods of programming are robust.

A. Programming Multiple Nonvolatile Memory Cells in Parallel Using Exact Placement

Figure 5 illustrates in flow diagram form a method of programming a number of memory cells in parallel to multiple states representing a pattern of bits. The method illustrated programs memory cells as close as possible to predefined states, whether those states are defined in terms of drain current or threshold voltage. The following discussion deals with the programming of four states associated with two data bits; however, the

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method is equally applicable to storage of an arbitrary number of bits of data by a single memory cell.

Briefly described, according to the present method all memory cells within a selected group are programmed simultaneously, regardless of their destination states; i.e., regardless of the amount of charge to be placed in each memory cell. An initial programming pulse is applied to all memory cells in the selected group. Afterward, each memory cell within the selected group is program verified to determine whether it has been programmed to its destination state. As used herein, program verification refers to the process of determining whether a defined amount of charge has been placed in a memory cell. No additional programming pulses are applied to those memory cells that program verify. If any memory cell within the selected group did not program verify, the wordline voltage of the programming pulse is increased. Another programming pulse is then applied to those memory cells which did not verify. The process of programming, verifying, and increasing the gate voltage continues until all memory cells verify or a maximum gate voltage is reached.

The programming method of Figure 5 steps the wordline voltage of each subsequent programming pulse rather than increasing the total programming duration of each subsequent programming pulse. The rationale for this programming strategy arises from the programming characteristics of nonvolatile memory cells. Figure 6 graphs memory cell threshold voltage V_t versus the log of programming time for four different

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gate voltages during programming. The gate voltages are relevant as an indication of the relative strength of the electric field across the gate oxide of the memory cell. Increasing gate voltage increases the strength of this electric field during programming. Curve 120 illustrates V_t versus time given a gate voltage of 8 volts. Curve 122 illustrates V_t versus time for a gate voltage of 9 volts. Gate voltages of 10 volts and 11 volts results in curves 124 and 126, respectively. All four curves 120, 122, 124 and 126 show threshold voltage increasing exponentially in the linear region to the left of curve 119. (The linear region is so named because when threshold voltage is plotted on a linear time scale in this region threshold voltage increases linearly.) That is to say, in the region to the left of line 119 the threshold voltage increases greatly given a small increase in programming pulse duration. This behavior is characteristic of nonvolatile memory cells that use hot electron injection for programming. Precise control of V_t is difficult when a memory cell is programmed in the linear region. Exact programming of a memory cell is easier in the saturated region of curves 120, 122, 124 and 126, which is to the right of curve 119. This is because in the saturated region, V_t increases more slowly, nearly logarithmically, with time. When programmed in the saturated region, all nonvolatile memory cells exhibit this logarithmic increase in V_t with increasing programming pulse duration regardless of whether they include a trapping dielectric or a floating gate, and regardless of the programming mechanism used.

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Programming of memory cells while operating in the saturated region is slow if the gate voltage is maintained constant and total programming pulse duration is increased. For example, curve 120 shows that a programming pulse of nearly 10 μ seconds duration is required to raise a memory cell's threshold voltage from 3 volts to 4 volts. Another 100 μ seconds programming pulse would be required to raise the threshold voltage from 4 volts to 5 volts. In contrast, curves 120, 122, 124 and 126 reveal nearly a one volt increase in V_t for each volt increase in the gate voltage when programming in the saturated region. As a result, memory cells can be more quickly programmed by increasing the gate voltage of each subsequent programming pulse than by maintaining a constant gate voltage and increasing total program pulse duration.

Precise control of memory cell programming via hot electron injection is achieved by choosing a sufficiently long initial pulse width, i.e. pulse duration, to ensure that programming occurs in the saturated region of the V_t versus time curve. The duration of a sufficiently long initial pulse width varies from device to device because of process variations. Despite this variation, the same initial pulse width can be used to program all devices in the saturated region if each device is appropriately trimmed after manufacture. One trimming technique that works well is trimming of the drain bias voltage level used during programming. Figure 7 illustrates V_t versus time curves at various drain bias voltage levels for one effective channel length. Other effective channel lengths will have a different family

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of curves. These curves show that programming in the saturated region for a selected initial pulse width is simply a matter of selecting an appropriate drain bias voltage, that is to say, a drain bias voltage level that forces the selected time to cause programming to occur in the saturated region.

Impact ionization induced bipolar turn-on voltage V_{Bii} limits the maximum drain bias voltage level that can be used while programming via hot electron injection. Turning on the parasitic bipolar transistor increases charge storage and makes precise placement of states difficult. Figure 9 illustrates the effect of V_{Bii} upon threshold voltage. For drain bias voltage levels less than V_{Bii} , increasing V_D only effects the linear region of the V_t versus time curve, as illustrated by the merging of curve for V_{D2} into the curve for V_{D1} . Maximum threshold voltage levels in the saturated region are unaffected by increased drain bias voltage levels. This is no longer the case when the drain bias voltage is above V_{Bii} . The V_t derived from a programming pulse of a constant duration at V_{D3} , with $V_{D3} > V_{Bii}$, will be greater than the V_t derived using V_{D1} and V_{D2} . For example, near V_{Bii} a difference of 0.1 volt in V_D can lead to a 0.2 - 0.25 volt difference in V_t .

Effective channel length, L_{eff} , effects the value of V_{Bii} . As the effective channel length increases, so does V_{Bii} . Effective channel length also effects the drain voltage at which the linear region transitions to the saturated region. Effective channel length varies as a result of the fabrication process. Thus, effective channel length, the voltage V_{Bii} , and the need to program within a reasonable time define a range of drain bias

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voltage levels appropriate for programming in the saturated region.

Devices may be trimmed after manufacture to program within this saturated region for a given minimum pulse duration. In one embodiment of flash memory device 20, acceptable values of the drain bias voltage range between 5.0 volts to 6.6 volts. Selecting an appropriate drain bias voltage level within this range requires characterization of effective channel lengths within a memory array during sort, subsequent to fabrication.

Given this explanation of memory cell programming behavior, now consider in detail the method of programming illustrated in Figure 5. Control engine 36 preferably begins by erasing memory array 22. This is because regardless of the number of bits stored by each memory cell, state 0 is achieved by erasure of the memory cell. Within flash memory arrays, all memory cells within a block are erased simultaneously. Stated another way, flash memory cells cannot be erased individually. It is possible, however, to program memory cells without prior erasure. Afterward, control engine 36 branches to step 92.

Control engine 36 prepares to program memory cells to states other than state 0 by initializing program variables in step 92. Control engine 36 sets the gate voltages of the memory cells to an initial programming level. The initial programming gate voltage level chosen depends upon the number of bits to be stored by each memory cell and the need to avoid overshooting the state immediately adjacent state 0. The source voltage is set to an initial value, such as ground, for example. During step 92 control

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engine 36 also sets the initial program pulse duration such that programming occurs within the saturated region. The drain bias voltage level to be used during programming has previously been trimmed to ensure that programming will occur in the saturated region given the initial pulse duration. For example, in one embodiment the initial programming pulse is 4 μ seconds. This done, control engine 36 branches to step 94.

Under the control of control engine 36, during step 94 a programming pulse is applied to all memory cells within the selected group, regardless of the state to which the memory cells are to be programmed. Control engine 36 does so by bringing the drain voltages V_D of the selected group of memory cells to a voltage level such that $V_{DS} = 5-7$ volts. Memory cells that are not to be programmed are protected from programming by coupling their bitlines to the source voltage level V_S so that $V_{DS} = 0$. In one embodiment, $V_S = 0-3$ volts.

The maximum size of the selected group of memory cells programmed at one time depends on a number of factors, and does not effect the present method of programming.

Control engine 36 stops the programming of the selected memory cells at step 96 by bringing the bitlines of the selected memory cells to V_S ; i.e., setting V_{DS} to 0 volts. Thus, it will be understood that the time duration of the programming pulse is controlled by the length of time $V_{DS} = 5-7$ volts.

To illustrate the effect of steps 92-96, assume that the selected group of memory cells includes memory cells 50, 52, and 54 of Figure 3. Assume

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further that memory cell 50 is to be programmed to state 0, memory cell 52 to state 1, and that state 3 is the destination state of memory cell 54. During step 92 common source line 76 is coupled to V_S . V_S may range between 0-3 volts. Word line 62 is coupled to the initial gate voltage level because it is coupled to the selected group of memory cells; e.g., cells 50, 52, and 54. In contrast, wordline 64 is coupled to V_S . Bitlines 66, 68, and 70 are coupled to V_S during step 92, thereby preventing programming of memory cells 50, 52 and 54 because $V_{DS} = 0$ volts. Control engine 36 brings bitlines 68 and 70 up to 5-7 volts above V_S during step 94, programming memory cells 52 and 54 simultaneously. After the period of time selected for the initial programming pulse has elapsed, control engine 36 ends the programming pulse at step 96 by bringing the voltage level coupled bitlines 68 and 70 to V_S .

Control engine 36 determines the success of the programming operation at step 98 via program verification. If a memory cell has reached its destination state, it is said to have verified. Conversely, if a memory cell has not yet been programmed to its destination state (as indicated by its drain current), then the memory cell is said to not have verified, or to have failed verification. During verification, each memory cell is compared to a reference representative of a destination state. For example, memory cell 52 is compared to a reference representative of state 1 and memory cell 54 is compared to a reference representative of state 3. Memory cell 52 will verify if its threshold voltage, drain current, or amount of current represents

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state 1, while memory cell 54 will verify if its threshold voltage, drain current, or amount of charge represents state 3. As a result of step 98, control engine 36 will receive a group of verify signals, one for each memory cell verified.

Verification complete, control engine 36 branches from step 98 to step 100. At step 100, control engine 36 inhibits further programming of memory cells that verified. Control engine 36 does so by coupling the bitlines associated with the verified memory cells to V_S prior to, and during, any subsequent programming pulses. Other mechanisms of inhibiting further programming of verified cells will be appropriate for array architectures differing from that of memory array 22. The particular mechanism for inhibiting further programming of cells that have reached their destination state does not effect the present method of programming. This done, control engine 36 branches to step 102.

Control engine 36 determines at step 102 if any further programming pulses should be applied to memory array 22. This determination is based upon examination of the verification signals. If any of these signal indicate that a memory cell has not yet been programmed to its destination state, then another programming pulse should be applied to memory array 22. Control engine 36 responds by branching to step 104.

Control engine 36 increases the voltage applied to memory cell gates by some amount, during step 104. Let us call that amount the "step size." The choice of step size depends upon the initial gate voltage, state

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width, and the need to prevent overshooting states. As used herein, "state width" refers to the range of drain currents, threshold voltages, or amount of charge defining a state. Larger state widths permit larger step size and thus require fewer programming pulses to program memory cells to the various states. To illustrate, consider Figure 9, which graphs the number of programming pulses required to program a group of memory cells in parallel versus state width. Figure 9 shows that the number of programming pulses required to program a group of multilevel memory cells decreases as state width increases.

In any case, control engine 36 increases the gate voltage by a step size up to a maximum, V_{\max} , at step 104. The maximum gate voltage is low enough to prevent damaging the memory cell and varies depending upon the process by which the memory cells are fabricated and the resulting strength of the electric field across the memory cell gate oxide. That done, control engine 36 branches to step 106.

During step 106, control engine 36 sets the time duration of the second and all subsequent programming pulses. Control engine 36 reduces the time duration of all subsequent pulses as compared to the time duration of the initial programming pulse to reduce the change in threshold voltage and drain current caused by increased total programming time, which could lead to overshooting states. The increase in threshold voltage from one programming pulse to the next arises from an increase in gate voltage and an increase in total program duration. To illustrate, assume

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that an initial programming pulse of 1 μ seconds at a gate voltage of 8 volts is applied to a memory cell and a second programming pulse is applied, which is one μ second in duration and has a gate voltage of 8.2 volts. Referring to Figure 6, the threshold voltage after the first programming pulse is 3.6 volts. An additional 1 μ second of programming at a gate voltage of 8 volts would increase V_t by approximately 0.25 volts and an additional 0.2 volt on the gate should increase V_t by only 0.2 volt. Thus, V_t would be increased by a total of 0.45 volts to 4.05 volts after the second programming pulse.

The relationship between the program pulse duration of all subsequent pulses to the initial pulse can be expressed mathematically as:

$$t_s = t_i/M$$

where:

t_s denotes the time duration of all pulses subsequent to the initial pulse;

t_i denotes the time duration of the initial programming pulse; and

M is the ratio of the duration of subsequent programming pulses to the duration of the initial programming pulse.

Selecting the ratio, M , is a function of the state width and gate voltage step size. In general, a large state width allows a large step size, which results in a small ratio M . Analogously, a small state width requires a small step size and a larger ratio M . Stated another way, to avoid overshooting states when using a large state width and large step size, the

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time duration of each subsequent pulse need not be greatly reduced. However, when the state width and gate voltage step size are small, the time duration of the subsequent programming pulses should be decreased rapidly to avoid overshooting states.

For another embodiment, during step 106 control engine 36 may reduce the duration of each subsequent program pulse as compared to the duration of the immediately preceding program pulse.

After control engine 36 has reduced and set the program pulse duration of subsequent programming pulses, control engine 36 branches to step 108. During step 108, control engine 36 examines the gate voltage level used during programming. If the gate voltage has reached a maximum value V_{MAX} and every memory cell within the selected group has not verified, then control engine 36 branches to step 110.

If the maximum gate voltage has not been reached, control engine 36 branches from step 108 to step 94 to apply another programming pulse to the selected group.

So long as a maximum number of pulses have not been applied, control engine 36 branches through steps 94-110, applying programming pulses until all memory cells have been programmed to their destination states. When that occurs, control engine 36 branches from step 102 to step 112 and programming is complete.

Once the gate voltage has reached its maximum value V_{MAX} , control engine 36 branches from step 108 to step 110. Step 110 permits control

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engine 36 to continue applying programming pulses even after the gate voltage has reached its maximum value until a maximum number of pulses have been applied. That maximum number is a design choice. Once the maximum number of pulses have been applied without successfully programming the selected group, control engine 36 branches from step 110 to step 111.

Control engine 36 notes the failure of the programming operation during step 111. Control engine 36 then branches to step 112, and the programming operation is over.

B. Programming Multiple Nonvolatile Memory Cells Independently Using Exact Placement

Figure 10 illustrates in flow diagram form a method of independently placing states in two memory cells. Stated another way, Figure 10 illustrates a method of programming multiple memory cells to different well-defined states independently of each other. For clarity, Figure 10 illustrates the programming of only two memory cells. Expansion of the method to larger number of memory cells will be apparent to one of ordinary skill in the art.

Programming begins during step 130 by selecting an initial voltage level to be applied to the gate, or wordline, of the first memory cell to be programmed. The initial wordline voltage level is selected such that the first memory cell will store the desired amount of charge representative of the first memory cell's destination state. That state may be defined in terms

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of a range of threshold voltages V_t , drain currents I_d , or amount of charge as discussed previously.

The initial wordline voltage chosen, a programming pulse is applied to the first memory cell. This is shown as step 132 in Figure 10. This done, control engine 36 branches to step 134.

Control engine 36 adjusts the wordline voltage level in step 134 to a level that will place the amount of charge desired within the next, or second, memory cell. Varying the wordline voltage level during programming thus provides a mechanism for placing differing discrete amounts of charge within memory cells.

Control engines 36 then applies a programming pulse to the second memory cell during step 136 using the wordline voltage level selected during step 134.

C. Program Verification of Nonvolatile Memory Cells Storing Multiple Bits That Have Been Exactly Placed

Up to this point sensing of data stored in a memory cell storing multiple bits and verification of that data have been described in general terms. They will now be discussed in greater detail because these processes are affected by the increase in the number of bits of data stored in a single memory cell.

Figure 11 illustrates in block diagram form circuit 32a, which is part of sensing circuitry 32. Circuit 32a senses and verifies the data stored in one nonvolatile memory cell storing multiple bits of data. Circuit 32a also

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controls the drain voltage applied to memory cell 22b during programming. The number of circuits 32a within sensing circuitry 32 determines the width of sensing circuit 32, and the number of memory cells that can be simultaneously read, programmed or verified.

Data stored within a memory cell of memory array 22, such as memory cell 22b, is sensed by applying a verify voltage to the cell gate, coupling approximately 1 volt to the drain, and coupling the source to ground, as is the common practice. Under these conditions, a current flows through the drain of memory cell 22b that is indicative of the threshold voltage of memory cell 22b and of the state to which memory cell 22b has been programmed. The drain of memory cell 22b is coupled to converter 142 to convert the state information of memory cell 22b into a bit pattern. The number of bits included in bit data 141 depends upon the number of states S memory cell 22b is capable of storing under the programming regime. The bit data 144 output from converter 142 is coupled to the rest of memory device 20 and to data pins 26.

The bit data 144 output from converter 142 is also coupled to cell verifier 146. Cell verifier 146 compares bit data 144 to the data that the external user wishes memory cell 22b to store. This data, program reference data 148 is stored in a data buffer, as is the common practice. Cell verifier 146 compares the data stored by memory cell 22b, represented by bit data 144, to program reference data 148. If bit data 144 matches program reference data 148, then cell verifier 146 brings VERIFY signal

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150 active, indicating that memory cell 22b has been successfully programmed to the desired state. Conversely, if bit data 144 is not the same as program reference data 148, then cell verifier 146 brings VERIFY 150 inactive, indicating to control engine 36 that memory cell 22b has not been programmed to the desired state.

Thus, methods and circuitry for programming nonvolatile memory cells have been described that place discrete amounts of charge in a single nonvolatile memory cell. Control of the wordline voltage level during programming controls the amount of charge placed in the memory cell. This allows multiple states to be defined in terms of charge amount, where each state represents a pattern of data bits. Thus, the method and circuitry described permit storage multiple bits of data in a single memory cell.

In the foregoing specification, the invention has been described with reference to specific exemplary embodiments thereof. It will, however, be evident that various modifications and changes may be made thereto without departing from the broader spirit and scope of the invention as set forth in the appended claims. The specification and drawings are, accordingly, to be regarded in an illustrative rather than a restrictive sense.

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CLAIMS

What is claimed is:

1. A method of programming a memory cell to a one of at least three amounts of charge comprising the step of:

a) applying a programming pulse having a programming voltage level to the memory cell, wherein an amount of charge stored by the memory cell is increased by increasing the programming voltage level.

2. The method of claim 1, wherein the memory cell is volatile.

3. The method of claim 1, wherein the memory cell is nonvolatile.

4. The method of claim 1, wherein the programming pulse has a duration sufficient to occur in a saturated region.

5. The method of claim 1, wherein the memory cell includes a bitline and a wordline.

6. The method of claim 5, wherein step a) includes coupling the programming voltage to the wordline and coupling a bitline voltage to the bitline.

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7. The method of claim 6 wherein the bitline voltage is less than an impact ionization bipolar turn-on voltage.

8. The method of claim 5 wherein the programming pulse has a duration, the method further comprising the step of:

b) trimming the bitline voltage such that the duration of the programming pulse causes the memory cell to program in a saturated region.

9. In a memory array including a first memory cell and a second memory cell, a method of placing a first amount of charge in the first memory cell and a second amount of charge in the second memory cell, the method comprising the steps of:

a) applying a first programming pulse to the first memory cell, the first programming pulse having a first programming voltage level; and

b) applying a second programming pulse to the second memory cell, the second programming pulse having a second programming voltage level different from the first programming voltage level.

10. The method of claim 9, wherein the memory cell is volatile.

11. The method of claim 9, wherein the memory cell is nonvolatile.

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12. The method of claim 9, wherein the first programming pulse has a duration sufficient to cause programming to occur in a saturated region.

13. The method of claim 9, wherein the nonvolatile memory array includes a first bitline coupled to the first memory cell and a first wordline coupled to the first memory cell.

14. The method of claim 13, wherein step a) includes coupling the first programming voltage to the first wordline and a first bitline voltage to the first bitline.

15. The method of claim 14, wherein the first bitline voltage is less than an impact ionization bipolar turn-on voltage.

16. The method of claim 14, wherein the first programming pulse has a first duration, the method further comprising the step of:

c) trimming the first bitline voltage such that the first duration of the first programming pulse causes the first memory cell to program in a saturated region.

17. In a memory array including a memory cell, a method of programming the memory cell to a selected state representing a pattern of data bits, the method comprising the steps of:

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- a) applying a programming pulse to the memory array, the programming pulse having a programming voltage level;
- b) generating a verify signal by determining whether the memory cell has been programmed to the selected state;
- c) increasing the programming voltage level if the verify signal indicates that the memory cell has not been programmed to the selected state; and
- d) repeating steps a) through c) until the verify signal indicates that the memory cell has been programmed to the selected state.

18. The method of claim 17, wherein the programming pulse has a program pulse duration having an initial value in step a) and wherein step c) further comprises setting the program pulse duration to a second value that is less than the initial value.

19. The method of claim 18 wherein the initial value of the program pulse duration is sufficient to cause programming of the memory cell to occur in a saturated region.

20. The method of claim 18, wherein the memory cell includes a bitline and the programming pulse includes a bitline voltage coupled to the bitline.

21. The method of claim 20, further comprising the step of:

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e) trimming the bitline voltage such that the initial duration of the programming pulse in step a) causes the memory cell to program in a saturated region.

22. The method of claim 17, wherein the selected state represents a pattern of two bits.

23. The method of claim 17, wherein the selected state represents a pattern of three bits.

24. The method of claim 17, wherein the selected state represents a pattern of 3.5 bits.

25. The method of claim 17, wherein the selected state represents a pattern of four bits.

26. The method of claim 17, wherein the selected state represents a noninteger number of bits.

27. The method of claim 17, wherein the selected state is represented by a range of threshold voltages.

28. The method of claim 17, wherein the selected state is represented by a range of drain currents.

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29. The method of claim 17, wherein the selected state is represented by an amount of charge.

30. In a memory array including a first memory cell and a second memory cell, a method of programming the first memory cell to a first state and programming the second memory to a second state, the first state representing a first pattern of bits and the second state representing a second pattern of bits, the first state having a first threshold voltage level, the second state having a second threshold voltage level that is greater than the first threshold voltage level, the method comprising the steps of:

a) applying a first programming pulse to the first memory cell, the first programming pulse having a first programming voltage level; and

b) applying a second programming pulse to the second memory cell, the second programming pulse having a second voltage level that is different than the first programming voltage level.

31. The method of claim 30, wherein the first memory cell is volatile.

32. The method of claim 30, wherein the first memory cell is nonvolatile.

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33. The method of claim 30, wherein the first selected state represents a pattern of three bits.

34. The method of claim 30, wherein the first selected state represents a pattern of 3.5 bits.

35. The method of claim 30, wherein the first selected state represents a pattern of a noninteger number of states.

36. The method of claim 30, wherein the selected state represents a pattern of two bits.

37. The method of claim 30, wherein the selected state represents a pattern of four bits.

38. In a memory array including a first memory cell and a second memory cell, a method of programming the first memory cell to a first state and programming the second memory cell to a second state, the first state representing a first pattern of a multiplicity of bits and the second state representing a second pattern of the multiplicity of bits, the method comprising the steps of:

a) applying a programming pulse to the memory array, the programming pulse having a programming voltage level;

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b) generating a first verify signal indicative of whether the first memory cell has been programmed to the first state;

c) generating a second verify signal indicative of whether the second memory cell has been programmed to the second state;

d) increasing the programming voltage level if the first verify signal indicates that the first memory cell has not been programmed to the first state or the second verify signal indicates that the second memory cell has not been programmed to the second state;

e) inhibiting further programming of the first memory cell if the first verify signal indicates that first memory cell has been programmed to the first state;

f) inhibiting further programming of the second memory cell if the second verify signal indicates that second memory cell has been programmed to the second state; and

g) repeating steps a) through f) until the first verify signal indicates that the first memory cell has been programmed to the first state and the second verify signal indicates that the second memory cell has been programmed to the second state.

39. The method of claim 38, wherein the multiplicity of bits equals two.

40. The method of claim 38, wherein the multiplicity of bits equals four.

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41. The method of claim 38, wherein the multiplicity of bits equals three.
42. The method of claim 38, wherein the multiplicity of bits equals 3.5.
43. The method of claim 38, wherein the multiplicity of bits is equal to a noninteger number.
44. The method of claim 38, wherein the first memory cell is volatile.
45. The method of claim 38, wherein the first memory cell is nonvolatile.
46. The method of claim 38, wherein the first and second states are each represented by a range of threshold voltages.
47. The method of claim 38, wherein the first state and the second state are each represented by a range of drain currents.
48. The method of claim 38, wherein the first state and the second state are each represented by an amount of charge.
49. The method of claim 38, wherein the memory array includes a first bitline coupled to the first memory cell, a second bitline coupled to the

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second memory cell, and a wordline coupled to the first memory cell and the second memory cell.

50. The method of claim 49, wherein step a) includes coupling the programming voltage to the wordline and a second voltage to the first bitline and a third voltage to the second bitline.

51. The method of claim 49, wherein the second voltage and third voltage are below an impact ionization bipolar turn on voltage.

52. The method of claim 49, wherein the programming pulse has a duration, the method further comprising the steps of:

h) trimming the second voltage and the third voltage such that programming of the first memory cell and the second memory cell occurs in a saturated region.

53. The method of claim 49, wherein step e) comprises coupling the first bitline to a fourth voltage during application of programming pulses to the memory array.

54. The method of claim 53, wherein the fourth voltage is ground.

55. The method of claim 38, wherein the programming voltage level ranges from a minimum of approximately 6 volts to a maximum of approximately 12 volts.

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56. In a memory array including a first memory cell and a second memory cell, a method of programming the first memory cell to a first state and programming the second memory cell to a second state, the first state representing a first pattern of a multiplicity of bits and the second state representing a second pattern of the multiplicity of bits, the method comprising the steps of:

- a) applying a programming pulse to the memory array, the programming pulse having a program voltage level and a duration, the duration having an initial value;
- b) generating a first verify signal indicative of whether the first memory cell has been programmed to the first state;
- c) generating a second verify signal indicative of whether the second memory cell has been programmed to the second state;
- d) increasing the program voltage level of the programming pulse by a step size and setting the duration to a subsequent value that is less than the initial value if the first verify signal indicates that the first memory cell has not been programmed to the first state or if the second verify signal indicates that the second memory cell has not been programmed to the second state;
- e) inhibiting further programming of the first memory cell if the first verify signal indicates that first memory cell has been programmed to the first state;

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f) inhibiting further programming of the second memory cell if the second verify signal indicates that second memory cell has been programmed to the second state; and

g) repeating steps a) through f) until the first verify signal indicates that the first memory cell has been programmed to the first state and the second verify signal indicates that the second memory cell has been programmed to the second state.

57. The method of claim 55, wherein each of the first state and the second state is represented by a range of threshold voltages.

58. The method of claim 56, wherein each of the first state and the second state is represented by a range of drain currents.

59. The method of claim 56, wherein each of the first state and the second state is represented by an amount of charge.

60. The method of claim 56, wherein the memory array is volatile.

61. The method of claim 56, wherein the memory array is nonvolatile.

62. The method of claim 56, wherein the multiplicity of bits equals three.

63. The method of claim 56, wherein the multiplicity of bits equals 3.5.

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64. The method of claim 56, wherein the multiplicity of bits equals two.

65. The method of claim 56, wherein the multiplicity of bits equals four.

66. The method of claim 56, wherein the multiplicity of bits equals a noninteger number.

67. The method of claim 56, wherein the memory array includes a first bitline coupled to the first memory cell, a second bitline coupled to the second memory cell and a wordline coupled to the first memory cell and the second memory cell.

68. The method of claim 56, wherein step a) includes coupling the programming voltage to the wordline, a second voltage to the first bitline and a third voltage to the second bitline.

69. The method of claim 68, wherein the second voltage and third voltage are below an impact ionization bipolar turn on voltage.

70. The method of claim 69, wherein the second voltage is less than 6.6 volts.

71. The method of claim 69, wherein the second voltage is greater than 5.1 volts.

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72. The method of claim 68, wherein the third voltage is less than 6.6 volts.

73. The method of claim 72, wherein the third voltage is greater than 5.1 volts.

74. The method of claim 68, wherein step e) comprises setting the second voltage equal to a fourth voltage.

75. The method of claim 74, wherein the fourth voltage is ground.

76. The method of claim 68, wherein step f) comprises setting the third voltage equal to a fifth voltage.

77. The method of claim 76, wherein the fifth voltage is ground.

78. The method of claim 56, wherein the programming voltage level ranges from a minimum of approximately 6 volts to a maximum of approximately 12 volts.

79. The method of claim 56, wherein the step size is between 0.1 volts and 0.5 volts.

80. The method of claim 56, wherein the duration is sufficient to program in a saturated region of the first memory cell and the second memory cell.

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81. A memory device comprising:
- a) a memory array including a first memory cell and a second memory cell, the first and second memory cells each storing discrete amounts of charge; and
 - b) programming circuitry for programming the first memory cell to a first discrete amount of charge by applying a first programming pulse having a first programming voltage to the first memory cell and programming the second memory cell to a second discrete amount of charge by applying a second programming pulse having a second programming voltage level to the second memory cell, the second programming voltage level differing from the first programming voltage level.
82. The method of claim 81, wherein the memory array is volatile.
83. The method of claim 81, wherein the memory array is nonvolatile.
84. The memory device of claim 81, wherein the memory array further includes:
- a) a first bitline coupled to the first memory cell; and
 - b) a first wordline coupled to the first memory cell.
85. The memory device of claim 84 wherein the programming circuitry includes:

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a) circuitry for coupling the first programming voltage to the first wordline and a second voltage to the first bitline.

86. The memory device of claim 85, wherein the first wordline is coupled to a gate of the first memory cell.

87. The memory device of claim 85, wherein the first bitline is coupled to a drain of the first memory cell.

88. A memory device comprising:

a) a memory array including a first memory cell and a second memory cell, the first and second memory cells each storing discrete amounts of charge; and

b) a control engine for programming of the first memory cell to a first range of charge and the second memory cell to a second range of charge by applying a first programming pulse having a first programming voltage level to the first memory cell and by applying a second programming pulse having a second programming voltage level to the second memory cell, the second programming voltage level being different than the first programming voltage level.

89. The memory device of claim 88 further comprising:

c) sensing and verification circuitry coupled to the nonvolatile memory array for generating a first verify signal and a second verify signal, the first verify signal indicating whether the first memory cell

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has been programmed within the first range of charge, the second verify signal indicating whether the second memory cell has been programmed within the second range of charge; and

wherein in response to the first verify signal indicating that the first memory cell has not been programmed within the first range of charge the control engine increases the first programming voltage level and applies again the first programming pulse to the first memory cell and wherein in response to the second verify signal indicating that the second memory cell has not been programmed within the second range of charge the control engine increases the second programming voltage level and applies again the second programming pulse to the second memory cell.

90. A computer system comprising:

- a) a processing means; and
- b) memory means coupled to the processing means, the memory means including:
 - 1) a memory array including a first memory cell, the first memory cell storing a first discrete amount of charge within a range of charge representing a first state, the first state representing a pattern of a multiplicity of bits;
 - 2) programming circuitry for programming the first memory cell to the first discrete amount of charge by applying a programming pulse having a wordline voltage level, the programming circuitry responding to a verify signal indicating that the first memory cell

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has not been programmed within a range of charge by increasing the wordline voltage level and applying another programming pulse to the first memory cell; and

3) verify circuitry for generating the verify signal indicative of whether the first memory cell has been programmed within the range of charge.

91. The computer system of claim 90 further comprising:

4) inhibiting means for inhibiting further programming of the first memory cell if the verify signal indicate that the first memory cell has been programmed within the range of charge.

92. A computer system comprising:

a) a central processing unit; and
b) memory device coupled to the central processing unit, the memory device including:
1) a memory array including a first memory cell and a second memory cell coupled to a wordline, the first memory cell storing a first amount of charge representative of a first state, the second memory cell storing a second amount of charge representative of a second state, the first state representing a first pattern of a multiplicity of data bits and the second state representing a second pattern of the multiplicity of data bits; and

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2) a control engine for programming of the first memory cell to the first state and the second memory cell to the second state by applying a programming pulse to the wordline, the programming pulse having a programming voltage level which the control engine increases if a first verify signal indicates that the first memory cell has not been programmed to the first state or a second verify signal indicates that the second memory cell has not been programmed to the second state, the control engine inhibiting further programming of the first memory cell if the first verify signal indicates that the first memory cell has been programmed to the first state and inhibiting further programming of the second memory cell if the second verify signal indicates that the second memory cell has been programmed to the second state.

93. A nonvolatile memory device comprising:

a) a memory array including a first nonvolatile memory cell and a second nonvolatile memory cell, the first and second memory cells each storing discrete amounts of charge; and

b) a control engine for programming of the first memory cell to a first range of charge and the second memory cell to a second range of charge by applying a programming pulse having a programming voltage level to the memory array, the control engine increasing the programming voltage level and applying another programming pulse to the memory array if a first verify signal or a second verify signal is inactive, the control engine inhibiting further programming of the first memory cell if the

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first verify signal is active and inhibiting further programming of the second memory cell if the second verify signal is active; and

c) sensing and verification circuitry coupled to the nonvolatile memory array for generating the first verify signal and the second verify signal, the sensing and verification circuitry bringing the first verify signal active to indicate that the first memory cell has been programmed within the first range of charge and bringing the first verify signal inactive to indicate that the first memory cell has not been programmed within the first range of charge, the sensing and verification circuitry bringing the second verify signal active to indicate that the second memory cell has been programmed within the second range of charge and bringing the second verify signal inactive to indicate that the second memory cell has not been programmed within the second range of charge.

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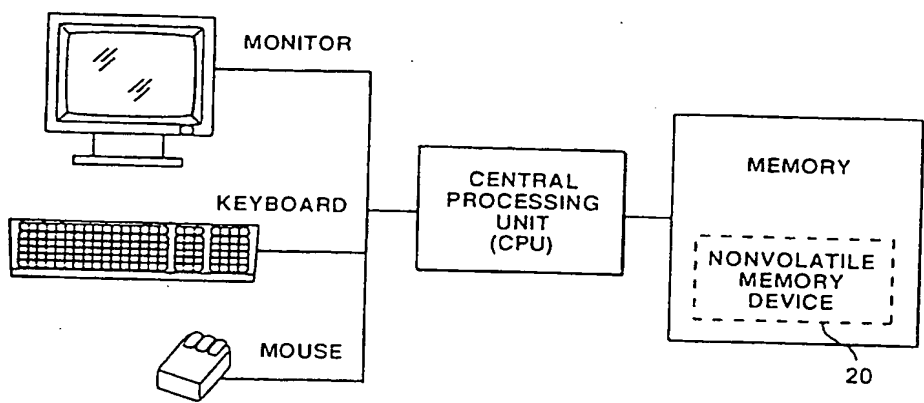


FIGURE 1

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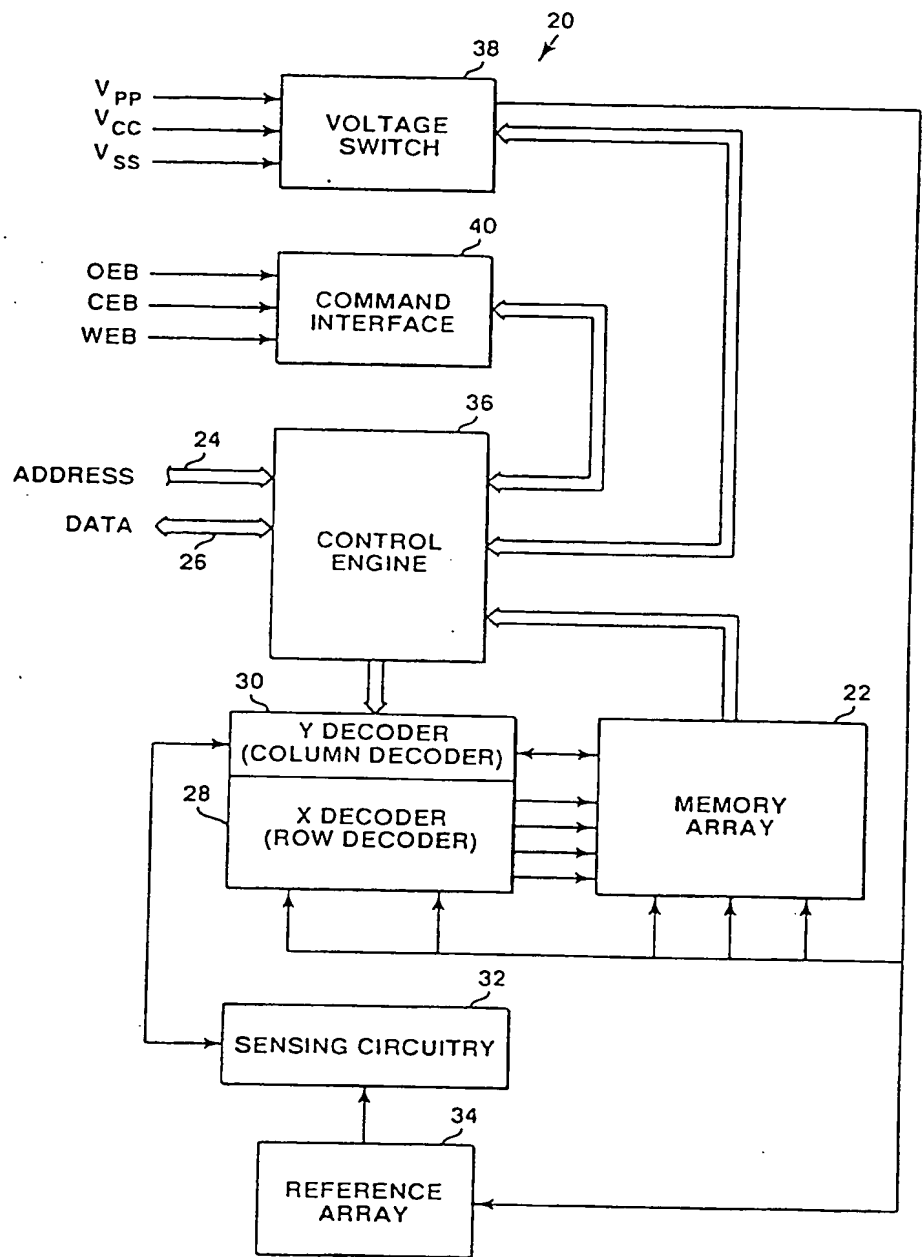
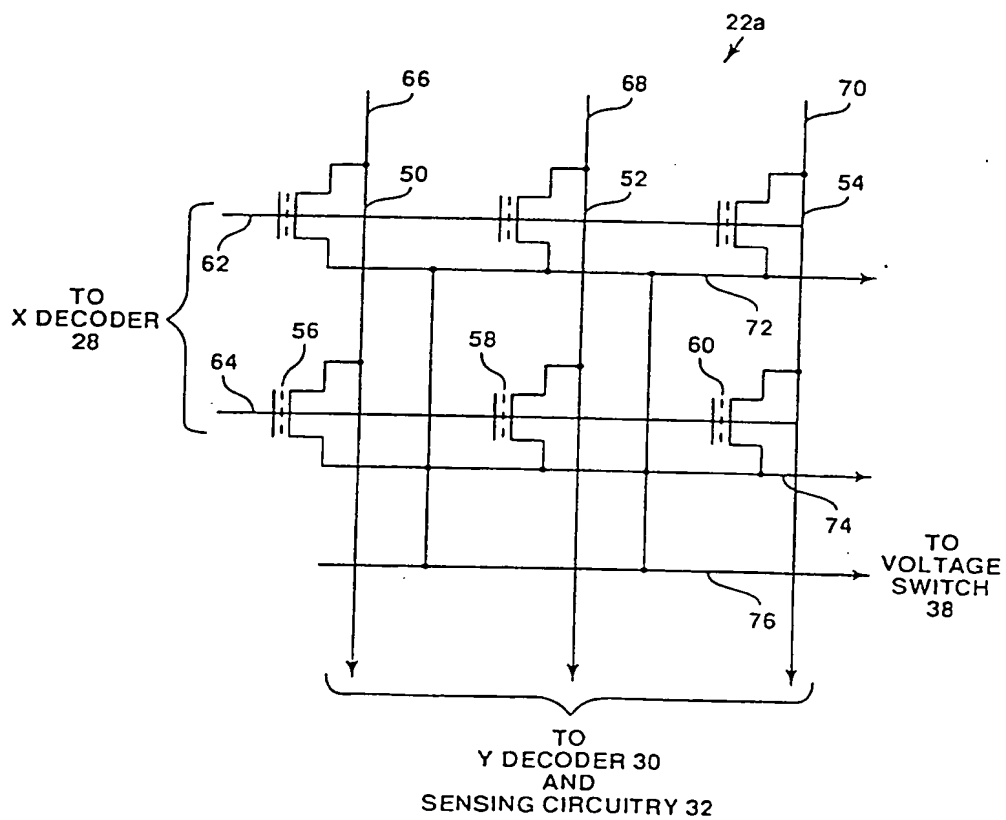


FIGURE 2

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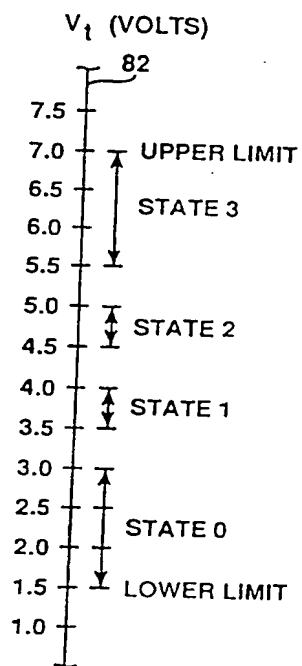


FIGURE 4A

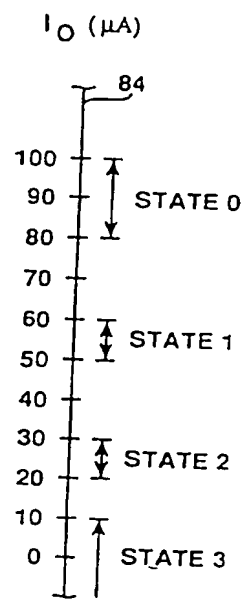


FIGURE 4B

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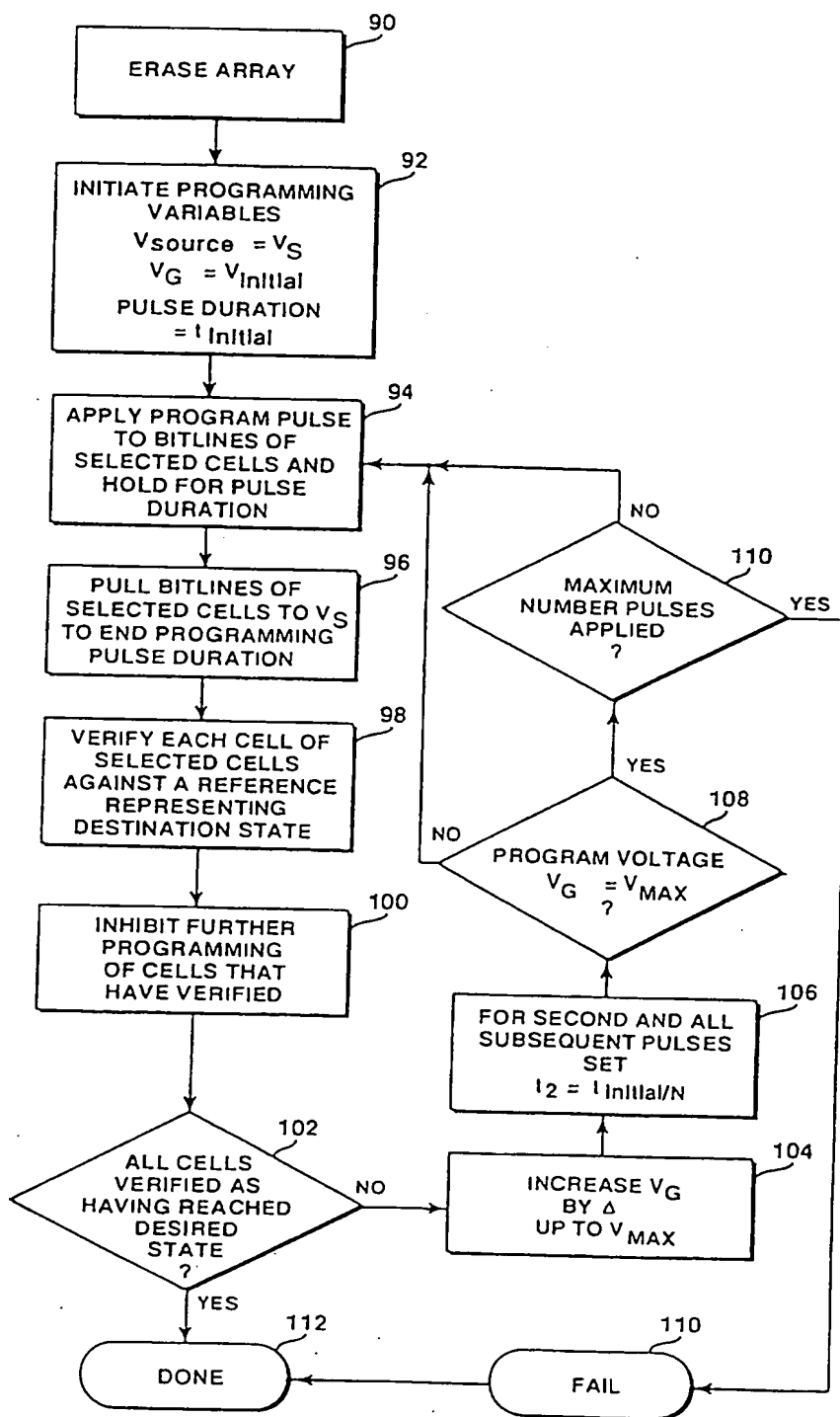


FIGURE 5

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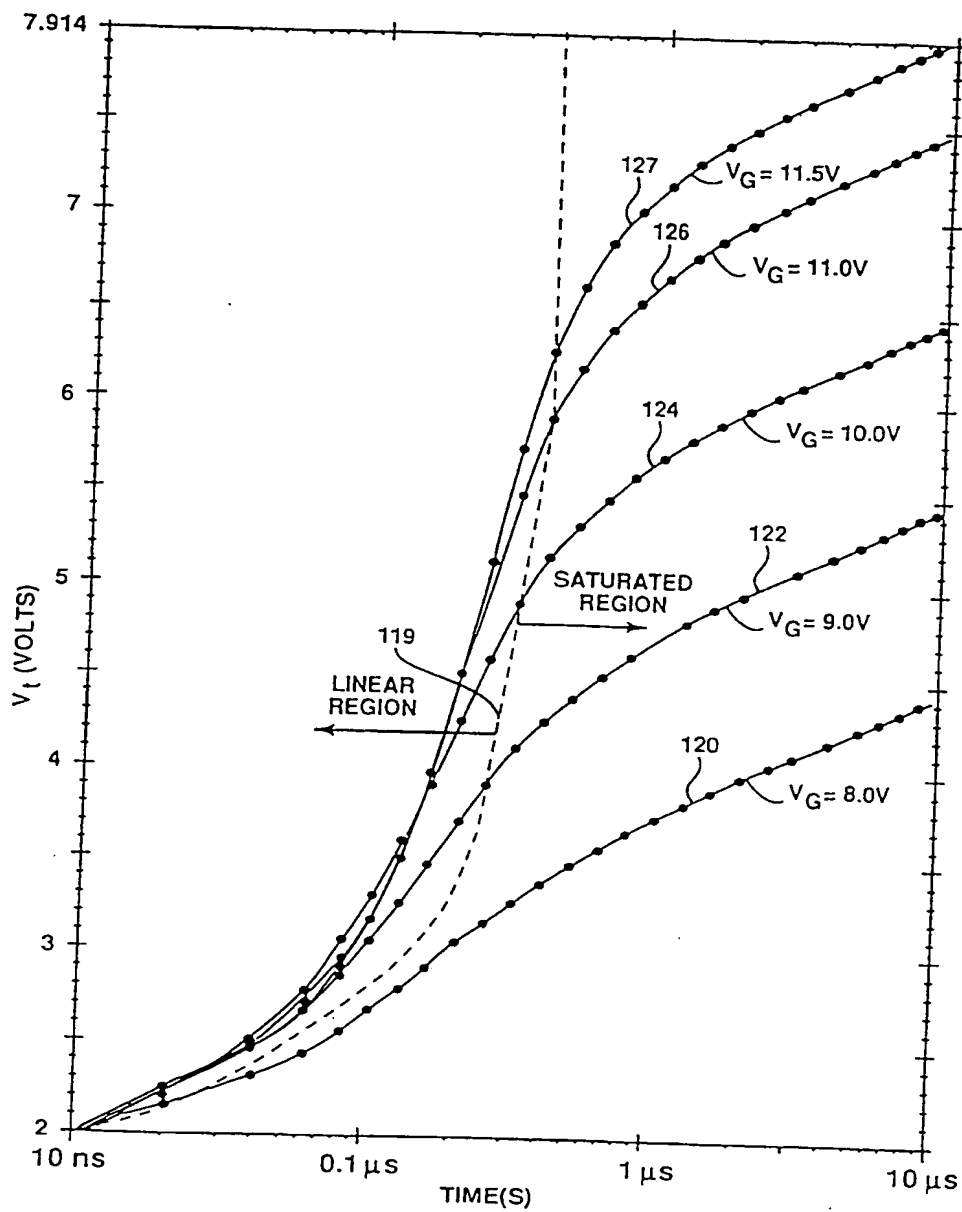


FIGURE 6

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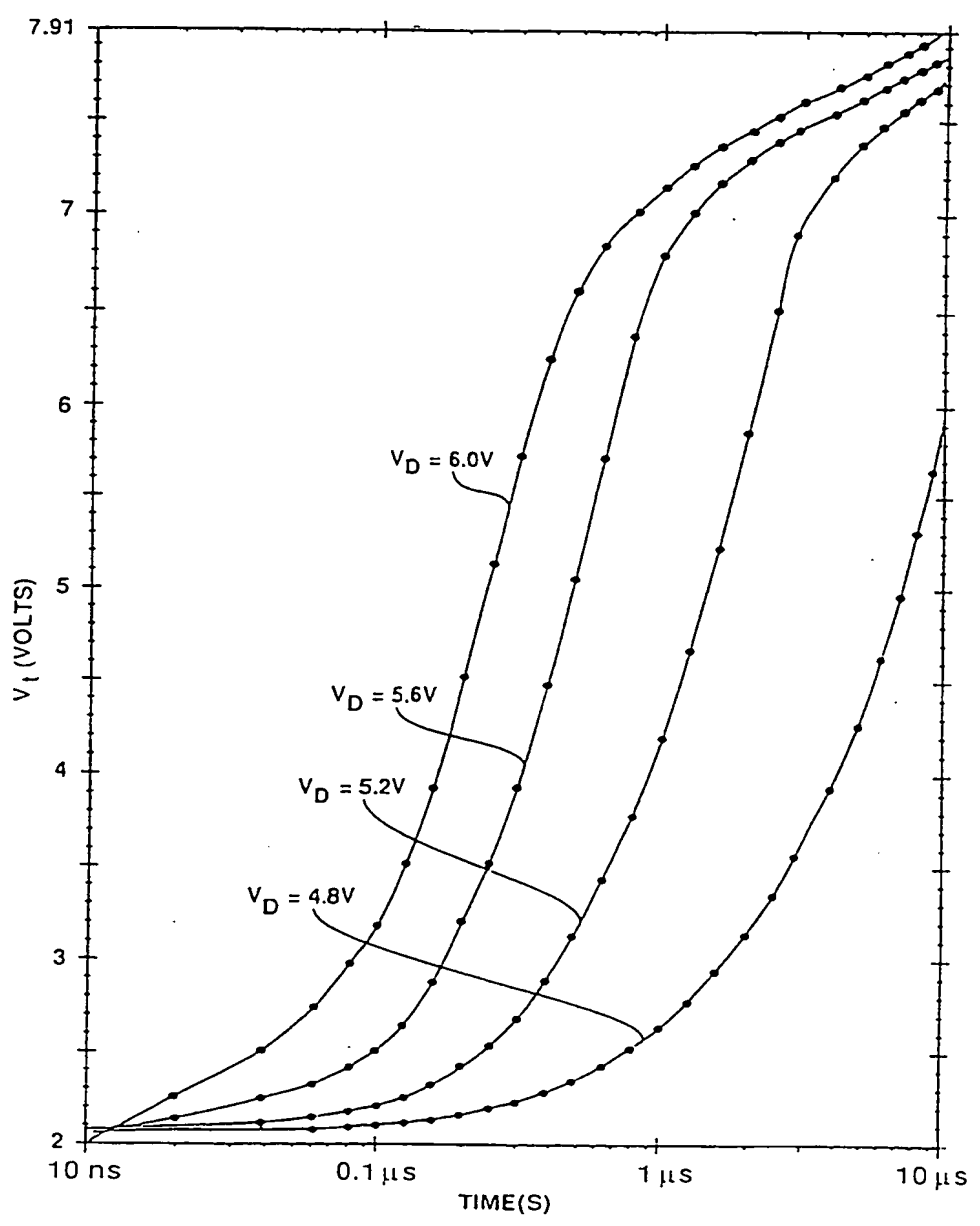


FIGURE 7

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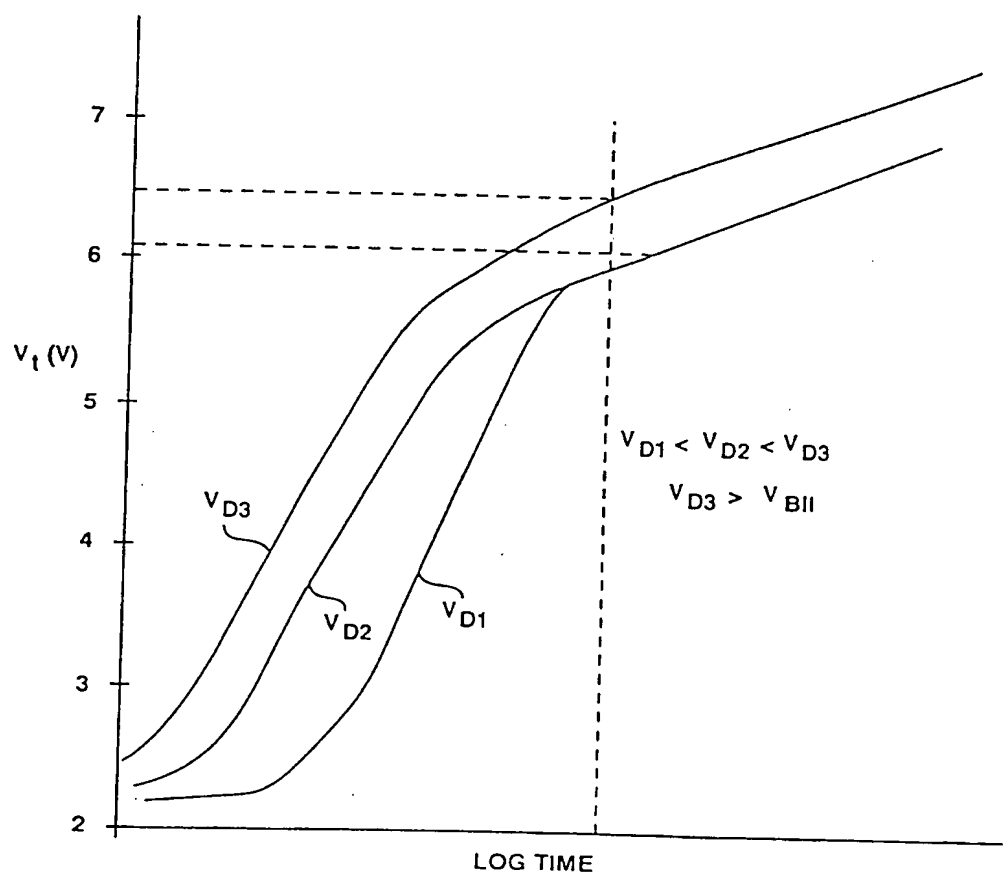


FIGURE 8

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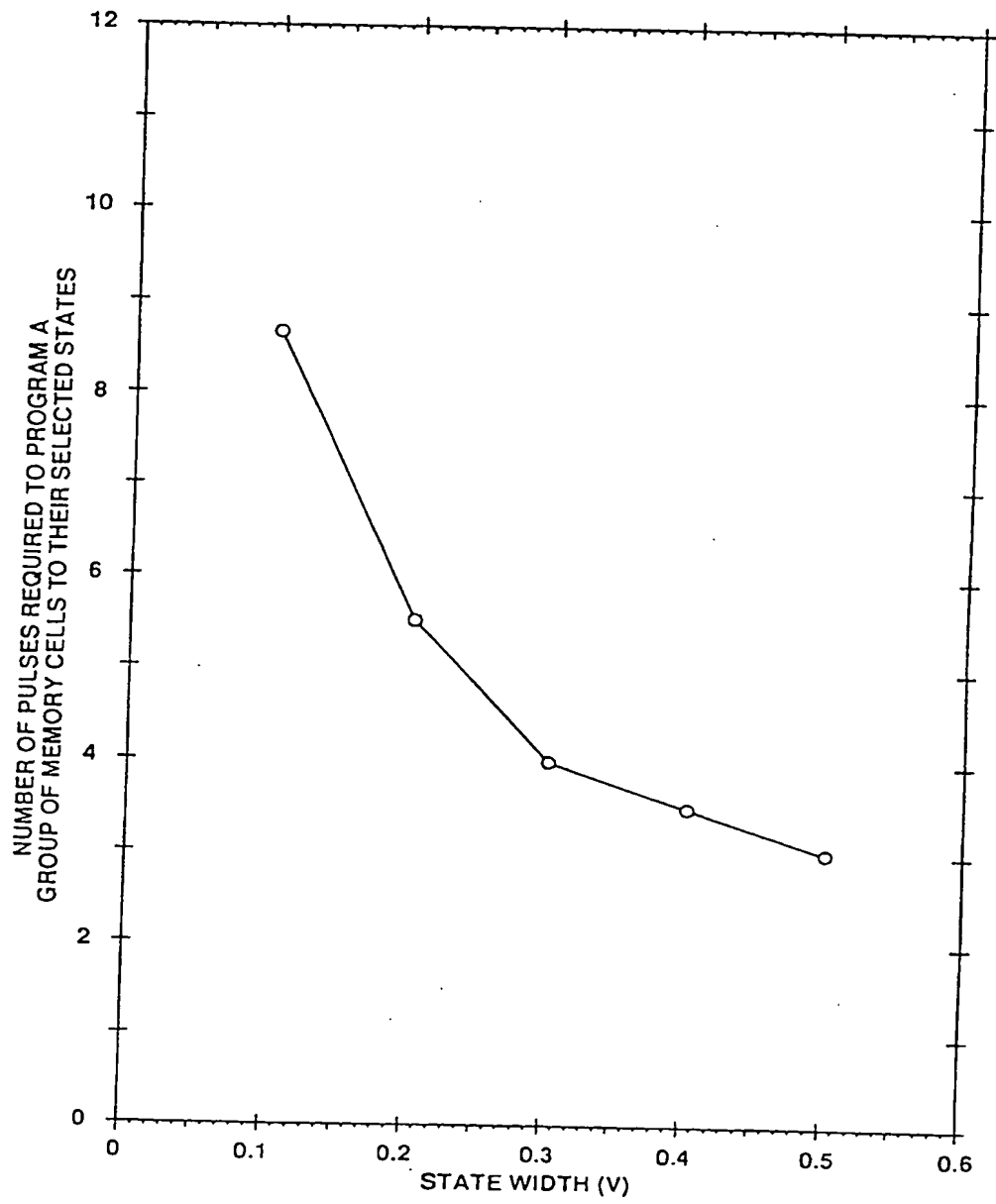


FIGURE 9

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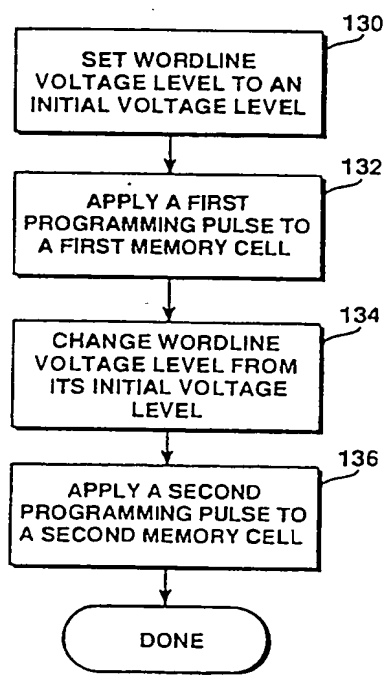


FIGURE 10

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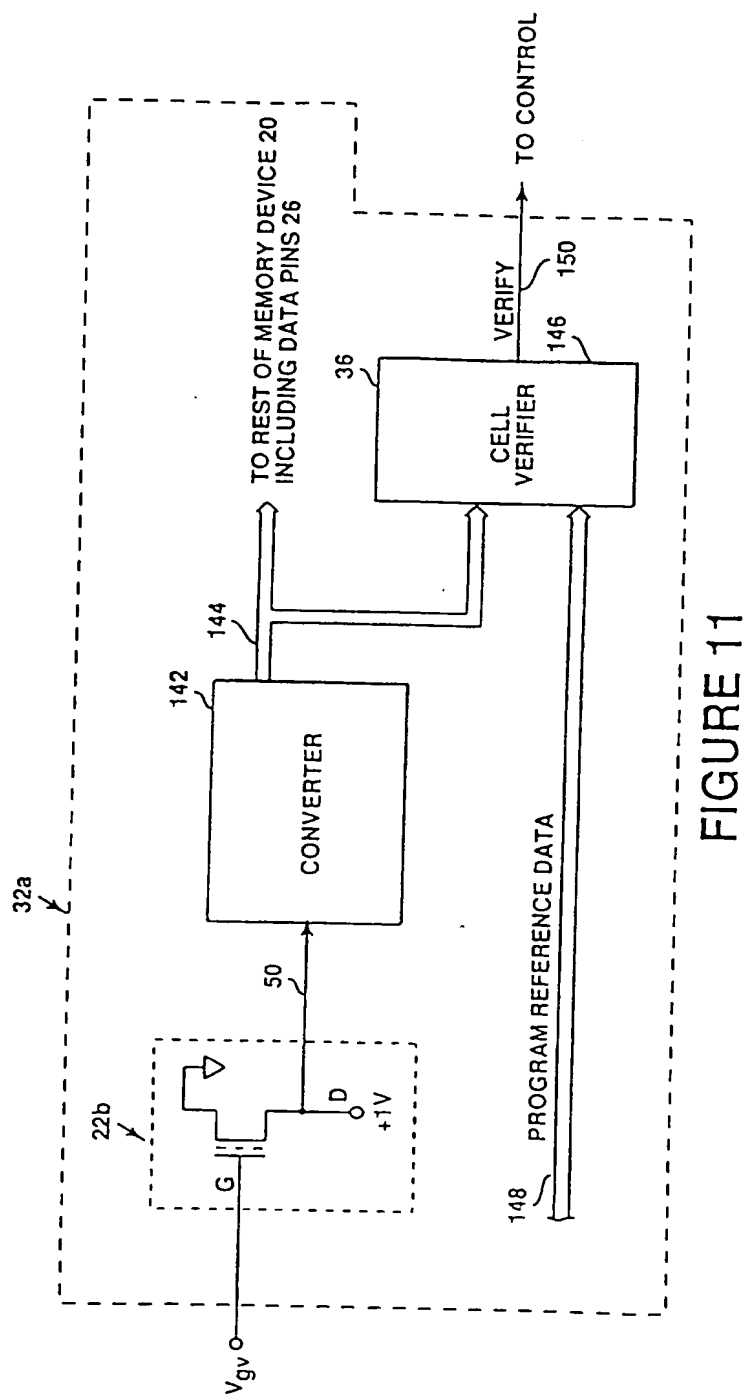


FIGURE 11

International Application No.

PCT/US 95/00152

IPC 6 G11C11/56 G11C27/00

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 6 G11C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	FR,A,2 246 022 (SIEMENS) 25 April 1975	1,2,4,5, 9,10,12, 81,82,88
A	see the whole document	6,22,23, 27,29, 85-87
X	WO,A,92 12519 (INFORMATION STORAGE DEVICES) 23 July 1992	1,3-5,8, 9,11-13, 27,81, 83,84, 88,89
	see the whole document	
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☒ Further documents are listed in the continuation of box C.

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Date of the actual completion of the international search

10 May 1995

Date of mailing of the international search report

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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT		
Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP,A,0 409 697 (GEMPLUS CARD INTERNATIONAL) 23 January 1991 see the whole document	1, 3-6
A	----	8
A	WO,A,90 12400 (SUNDISK CORPORATION) 18 October 1990 cited in the application see page 40, line 26 - page 41, line 31 ----	1,3,5,6, 8,17,27
X	PATENT ABSTRACTS OF JAPAN vol. 7 no. 23 (P-171) [1168] ,29 January 1983 & JP,A,57 176598 (SANYO DENKI) see abstract ----	1
A	EP,A,0 130 614 (HITACHI) 9 January 1985 see the whole document -----	1

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No

PCT/US 95/00152

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
FR-A-2246022	25-04-75	DE-A- 2348961	15-05-75
		AT-B- 342342	28-03-78
		BE-A- 820448	27-03-75
		CH-A- 582938	15-12-76
		GB-A- 1486912	28-09-77
		JP-A- 50062333	28-05-75
		LU-A- 71005	17-04-75
		NL-A- 7412832	02-04-75
		SE-B- 402998	24-07-78
		SE-A- 7412226	01-04-75
WO-A-9212519	23-07-92	US-A- 5220531	15-06-93
		EP-A- 0565622	20-10-93
		JP-T- 6504156	12-05-94
EP-A-409697	23-01-91	FR-A- 2650109	25-01-91
		CA-A,C 2021585	21-01-91
		DE-D- 69003321	21-10-93
		DE-T- 69003321	13-01-94
		ES-T- 2047286	16-02-94
		JP-A- 3214779	19-09-91
		US-A- 5394359	28-02-95
WO-A-9012400	18-10-90	EP-A- 0539358	05-05-93
		JP-T- 4507320	17-12-92
		US-A- 5172338	15-12-92
		US-A- 5163021	10-11-92
EP-A-130614	09-01-85	JP-C- 1849047	07-06-94
		JP-A- 60013398	23-01-85
		CA-A- 1224567	21-07-87
		DE-A- 3485555	16-04-92
		US-A- 4709350	24-11-87

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